REMARKS

This is intended as a full and complete response to the Office Action dated January 20, 2004 having a shortened statutory period for response set to expire on April 20, 2004. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-28 have been presented for examination. Claims 7-11, 18, and 25-28 have been previously canceled. New claims 29-38 have been previously added. Accordingly claims 1-6, 12-17, and 19-38 remain pending in the application.

Claim Rejections - 35 USC § 102 (Ang)

Claims 1-6, 12-14, 19-24, and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by *Ang* (U.S. Pub. No. 2003/0079085).

As per claims 1, 12, and 19, Examiner submits that *Ang* teaches a method of managing cache in a shared memory multiple processor computer system:

Executing, by a processor, a cache purge instruction that configures the processor to purge a cache line from the processor and send the cache line to at least one of a plurality of processors in the shared memory multiple processor computer system to update the at least on of a plurality of processors (citing page 2, paragraph 25, lines 1-15 of *Ang*).

Applicants respectfully submit, however, that the operations described in the cited portion of *Ang* do not teach executing a cache purge instruction, as claimed in claims 1, 12, and 19, of the present application. Rather *Ang* teaches monitoring store instructions issued from multiple nodes/processors, in an effort to aggregate modifications made by these store instructions to a common cache line into a single write to main memory. Not only are the operations described by *Ang* different than those claimed, but the operations described by *Ang* are performed by components of a *memory controller* 106, not a processor, as claimed.

Accordingly, Applicants submit that claims 1, 12, 19, and 34 are patentable over *Ang* and respectfully request removal of this rejection with respect to these claims and those that depend therefrom.

Claim Rejections - 35 USC § 102 (Yates)

Claims 29, and 35 are rejected under 35 U.S.C. 102(e) as being anticipated by *Yates et al.* (U.S. Patent No. 6,549,959).

As per claims 29, and 35, the Examiner submits that *Yates* teaches a method of managing cache in a shared memory multiple processor computer system, comprising:

executing, by a processor, a cache purge instruction that configures the processor to purge a cache line from the processor and send the cache line to at least one of a plurality of processors in the shared memory multiple processors (col. 31, lines 41-42, data in the cache are current mean that data have been purged and updated), wherein the cache purge instruction updates all caches in the computer system and marks a state of all updated cache line as shared (citing col. 31, lines 41-49 of *Yates*).

Applicants respectfully submit, however, that the cited portion of *Yates* does not teach executing, by a processor, a cache purge instruction that configures the processor to purge a cache line or send the cache line to at least one of a plurality of processors in the shared memory multiple processors, as claimed. Rather, as described in col. 31, lines 14-62 (which includes the section cited by the Examiner) the method of transferring data into processor cache described in *Yates*, involves conventional transferring of data from main memory to processor caches in a manner analogous with the standard MESI (Modified, Exclusive, Shared, Invalid) cache protocol, but does not teach sending a cache line from the cache of one processor to the cache of another processor, as claimed.

Claim Rejections - 35 USC § 103 (Ang and AAPA)

Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Ang*, and further in view of *AAPA*.

As per claim 30, the Examiner submits that *Ang* teaches a method of managing cache in a shared memory multiple processor computer system, comprising:

Executing, by a processor, a cache purge instruction that configures the processor to purge a cache line from the processor and send the cache line to at least one of a plurality of processors in the shared memory multiple processors, wherein the

cache purge instruction updates all caches in the computer system (page 2, paragraph 25, lines 1-16).

The Examiner states, however, that *Ang* fails to teach marking a state of all updated cache line as temporarily invalid, buts cites portions (page 8, paragraph 30, lines 6-8) of a reference identified only as "*AAPA*" as teaching when an entry in the cache is changed or modified, the directory temporary invalidates the respective directory entry corresponding to the cache line. Applicants were unable to find a complete citation to this reference in the Office Action or the attached Notice of References Cited.

Nonetheless, Applicants submit, however, that *Ang* does not teach executing a cache purge instruction, as claimed in claim 30, for reasons described above with reference to claims 1, 12, and 19. Therefore, Applicants submit, based on the limited information available from the Office Action, that the combination of references suggested by the Examiner fails to teach the elements of the current application, as claimed in claim 30. Accordingly, Applicants request removal of this rejection with respect to this claim.

Claim Rejections - 35 USC § 103 (Ang and Yates)

Claims 15-16, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Ang*, and further in view of *Yates*.

As per claims 15-16, and 34, the Examiner submits that *Ang* teaches a computer system, comprising a shared memory and at least two processors wherein each processor is associated with at least one level of cache and wherein each processor, when executing a cache purge instruction and send the cache line to at least one other processor in the computer system to up date the at least one other processor (page 2, paragraph 25, lines 1-16).

The Examiner states, however, that *Ang* fails to teach the cache purge instruction is referenced to at least five fields and one of the at least five fields indicates how the state of the updated cache(s) will be marked, but relies on *Yates* (col. 30, lines 58-67) as teaching this claimed element.

Applicants submit, however, that *Ang* does not teach executing a cache purge instruction, as claimed in claims 15-16, and 34, for reasons described above with reference to claims 1, 12, 19, and 30. Further, Applicants submit that the cited portions of *Yates*, fail to teach that a purge instruction is referenced to at least five fields and one of the at least five fields indicates how the state of the updated cache(s) will be marked, as claimed, or a purge instruction at all.

Therefore, Applicants submit that the combination of references suggested by the Examiner fails to teach the elements of the current application, as claimed in claims 15-16 and 34. Accordingly, Applicants request removal of this rejection with respect to these claims.

Claim Rejections - 35 USC § 103

Claims 31-33, and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Ang*, and further in view of *Liu* (US 5,210,848).

As per claims 31, and 36, the Examiner states that *Ang* teaches a method of managing cache in a shared memory multiple processor computer system:

executing, by a processor, a cache purge instruction that configures the processor to purge a cache line from the processor and send the cache line to at least one of a plurality of processors in the shared memory multiple processor computer system to update the at least on of a plurality of processors (page 2, paragraph 25, lines 1-15).

The Examiner states, however, that *Ang* fails to teach wherein the cache purge instruction updates only one cache at a designated processor of the plurality of processors then marks a state of the cache line updated as exclusive at the designated processor and marks a state of the cache line as temporarily invalid at the processor executing the instruction, but relies on *Liu* as teaching this element.

Applicants submit, however, that *Ang* does not teach executing a cache purge instruction, as claimed in claims 31-33, and 36-38, for reasons described above with reference to claims 1, 12, 19, and 30. Further, Applicants fail to see how the cited portions of *Liu* (claim 2) teach wherein the cache purge instruction updates only one

cache at a designated processor of the plurality of processors then marks a state of the cache line updated as exclusive at the designated processor and marks a state of the cache line as temporarily invalid at the processor executing the instruction, that a purge instruction is referenced to at least five fields and one of the at least five fields indicates how the state of the updated cache(s) will be marked, as claimed, or a purge instruction at all.

Therefore, Applicants submit that the combination of references suggested by the Examiner, fails to teach the elements of the current application, as claimed in claims 31-33, and 36-38. Accordingly, Applicants submit these claims are patentable over the suggested combination and request removal of this rejection with respect to these claims.

Conclusion

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,

Gero G. McClellan
Registration No. 44,227
MOSER, PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Attorney for Applicant(s)